Page 1, paragraph 3:

A1

FIG. 15 shows a conventional RF circuit. FIG. 16 shows a plan configuration of an RF semiconductor device in which the RF circuit shown in Fig. 15 is implemented in a substrate. In FIG. 16, the same components as shown in FIG. 15 are designated by the same reference numerals. Specifically, the RF circuit comprises a DC blocking capacitance 307, a register 308, a drain terminal 313, a gate terminal 314 and a source terminal 315.

Page 7, paragraph 3:

A2

FIGS. 2A, 2B and 2C are structural cross-sectional views illustrating the individual process steps of a method for fabricating the microstrip line according to the first embodiment;

Page 7, paragraph 6:

A3

FIGS. 5A, 5B and 5C are structural cross-sectional views illustrating the individual process steps of a method for fabricating the microstrip line according to the second embodiment;

Page 8, paragraph 5:

A4

FIGS. 10A, 10B, 10C, and 10D are structural cross-sectional views illustrating the individual process steps of a method for fabricating the microstrip line according to the third embodiment;

Page 8, paragraph 6:

A5

FIGS. 11A, 11B, 11C and 11D are structural cross-sectional views illustrating the individual process steps of a method for fabricating the microstrip line according to the third embodiment;

Page 8, paragraph 7:

A6

FIGS. 12A, 12B, 12C and 12D are structural cross-sectional views illustrating the individual process steps of a method for fabricating the microstrip line according to the third embodiment;

Page 8, paragraph 8:

A7

FIGS. 13A, 13B and 13C are structural cross-sectional views illustrating the individual process steps of a method for fabricating the microstrip line according to the third embodiment;

Page 9, paragraph 1:

A8

FIGS. 14A, 14B and 14C are structural cross-sectional views illustrating the individual process steps of a method for fabricating the microstrip line according to the third embodiment;

Page 12, paragraph 2 continuing onto page 13:

A9

Next, as shown in FIG. 3B, the third resist film 23 shown in Fig. 3A is removed and an unwanted portion of the Au layer in the upper part of the multilayer structure composing the second-layer forming layer 16A shown in Fig. 3A is removed by using an etchant composed of potassium iodine (KI). Subsequently, an unwanted portion of the Ti layer in the lower part of the multilayer structure composing the second-layer forming layer 16A is removed by using hydrogen fluoride (HF), whereby the second-layer forming layer 16A is patterned into the second layer 16 of the linear conductor layer 14. Thereafter, the second resist film 22 shown in Fig. 3A is removed by using a resist remover and then the protective insulating film 18 composed of a silicon dioxide is deposited entirely over the dielectric layer 13 so as to cover the linear conductor layer 14.

Page 14, Paragraph 3 continuing onto page 15:

A10

Although the protective insulating film 18 composed of the silicon dioxide has been filled in the space between the wider portion 14b of the linear conductor layer 14 and the dielectric layer 13 in order to protect the strip line, it is preferred not to fill the protective insulating film 18 in terms of operation characteristics. In the case of filling the protective insulating film 18, therefore, a low dielectric film having a relatively low dielectric constant such as an organic material composed of, e.g., benzocyclobutene, DUROID, or a polymide film is use preferably.

Page 18, paragraph 1:

A11

Referring to Figures 5A-5C, 6A and 6B, a description will be given to a method for fabricating the microstrip line thus constituted.

Page 19, paragraph 1:

A12

Next, as shown in FIG. 5C, the narrower-portion formation region of the dielectric layer 33 is exposed by lifting off the first resist film 41 shown in Fig. 5B. Then, the first layer 35 of the linear conductor layer composed of WSiN is deposited by RF sputtering. Thereafter, a second resist film 42 is coated on the deposited first layer 35 and formed into a line pattern with a width of about 5 μm by lithography so as to include the narrower-portion formation region. Subsequently, the first layer 35 is etched back by using the formed second resist film 42 as a mask and using CF_4 to be formed into a pattern including the narrower portion 34a. Thereafter, sintering is performed in an oxygen ambient at a temperature of about 450 °C to recrystallize the dielectric layer 33 and thereby increase the dielectric constant of the dielectric layer 33.

Page 20, paragraph 1:

A13

Next, as shown in FIG. 6B, the third resist film 43 shown in Fig. 6A is removed and an unwanted portion of the Au layer in the upper part of the multilayer structure of the second-layer forming layer 36A is removed by using an etchant composed of KI. Subsequently, an unwanted portion of the Ti layer in the lower part of the multilayer structure of the second-layer forming layer 36A shown in Fig. 6A is removed by using hydrogen fluoride, whereby the second-layer forming layer 36A is patterned into the second layer 36 of the linear conductor layer 34.

Page 23, paragraph 4 continuing onto page 24:

A14

Although the second embodiment has used GaAs in the substrate 31, an inorganic material composed of a glass material such as Si or quartz or of alumina or an organic material composed of polystyrene or TEFLON may also be used instead.

Page 24, paragraph 4:

A15

A third embodiment of the present invention will be described with reference to Figures 7-14C inclusive.

Page 28, paragraph 2:

A16

FIGS. 10A to 10D, 11A to 11D, 12A to 12D, 13A to 13C and 14A to 14C show the cross-sectional structures of the RF semiconductor device according to the third embodiment in the individual process steps. For the sake of simplicity, the description will be given to a method for forming, over the substrate 211, a region different from the region 50 shown in FIG. 7 and including a FET formation region 1 in which a FET as an amplifying element is to be formed and a line formation region 2 in which a microstrip line is to be formed, as shown in FIG. 10A.

Page 29, paragraph 1:

A17

Next, mesa etching is performed with respect to the FET formation region 1. Subsequently, a first resist film 251 is coated on the substrate 211 and formed into a line pattern 251a with a width of about 0.2 μm, which is for determining the gate length of the FET, in the FET formation region 1 by lithography using a phase shifting method. Thereafter, a first protective insulating film 212 composed of SiO_2 with a thickness of about 0.2 μm is deposited over the entire surface of the substrate 211 by ion beam sputtering using the first resist film 251 as a mask.

Page 29, paragraph 2:

A18

Next, as shown in FIG. 10B, the first resist film 251 shown in Fig. 10A is lifted off and then a second protective insulating film 213 composed of SiN with a thickness of about 0.3 μm is formed by CVD entirely over the substrate 211 including the first protective insulating film 212.

Page 29, paragraph 4 continuing onto page 30:

A19

Next, as shown in FIG. 10D, a second resist film 252 covering the FET formation region 1 shown in Fig. 10A is formed. Then, a layer 215B forming the

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second layer of the ground electrode and composed of Au with a thickness of about 2.5 μm is formed by plating. Subsequently, a layer 215C forming the third layer of the ground electrode and composed of a multilayer structure of Pt with a thickness of about 0.2 μm and Ti with a thickness of about 0.02 μm is formed by vapor deposition again.

Page 30, paragraph 1:

A20

Next, as shown in FIG. 11A, the second resist mask 252 is removed and the layer 215A forming the first layer in the FET formation region 1 is removed therefrom by using a KI etchant and hydrogen fluoride, whereby a ground electrode 215 composed of the first-layer forming layer 215A, the second-layer forming layer 215B, and the third-layer forming layer 215C is formed in the line formation region 2. Subsequently, a third protective insulating film 216 composed of SiN with a thickness of about 0.3 μ m is deposited over the entire surface of the substrate 211.

Page 30, paragraph 2:

A21

Next, as shown in FIG. 11B, a third resist mask 253 having an opening pattern in the line formation region 2 is formed on the third protective insulating film 216 by lithography. Subsequently, Reactive Ion Etching (RIE) etching is performed with respect to the third protective insulating film 216 by using the third resist film 253 as a mask, thereby exposing the ground electrode 215.

Page 30, paragraph 3 continuing onto page 31:

A22

Next, as shown in FIG. 11c, the third resist film 253 shown in Fig. 11A is removed and then a dielectric layer 217 composed of STO with a thickness of about 0.5 μm is deposited entirely over the substrate 211 including the line formation region 2 by RF sputtering for which the substrate temperature is adjusted to about 300 °C.

Page 31, paragraph 1:

A23

Next, as shown in FIG. 11D, the portion of the dielectric layer 217 included in

A23 cancel

the FET formation region 1 shown in Fig. 11A is removed by a milling method using a fourth resist mask 254 covering the line formation region 2 of the dielectric layer 217.

Page 31, paragraph 2:

A24

Next, as shown in FIG. 12A, the fourth resist mask 254 shown in Fig. 11D is removed and then a layer 218A forming the first layer of the linear conductor layer and composed of WSiN with a thickness of about 0.1 μm is deposited over the entire surface of the substrate 211 by RF sputtering. Thereafter, the dielectric layer 217 is recrystallized by performing sintering in an oxygen ambient at a temperature of about 450 °C.

Page 32, paragraph 2:

A25

Next, as shown in FIG. 12D, the sixth resist film 256 shown in Fig. 12C is removed and then a seventh resist film 257 having opening patterns for exposing the source/drain formation regions of the FET formation region 1 is formed on the substrate 211 by lithography. Subsequently, etching is performed with respect to the first protective insulating film 212 by using hydrogen fluoride and using the formed seventh resist film 257 as a mask, thereby exposing the source/drain formation regions of the top surface of the substrate 211.

Page 36, paragraph 2:

A26

Although the space between the wider portion 225b of the linear conductor layer 225 and the dielectric layer 217 is filled with the fourth protective insulating film 222 composed of SiN in the present embodiment, the space may be filled preferably with a material having a lower dielectric constant such as an inorganic thin film composed of, e.g., SiO_2 or with an organic thin film composed of BCB, DUROID, or the like.